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| **Course Title** | Low-Power Digital Integrated Circuits |
| **Semester/Year** | F2020 |
| **Lab No** | 03 |
| **Instructor Name** | Dr. Andy Ye |
| **Section No** | 06 |

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| **Submission Date** | 11/15/2020 |
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| **Name** | **Student ID** | **Signature\*** |
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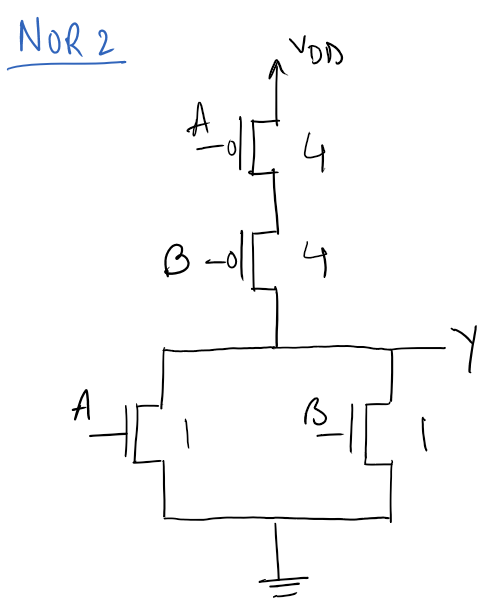
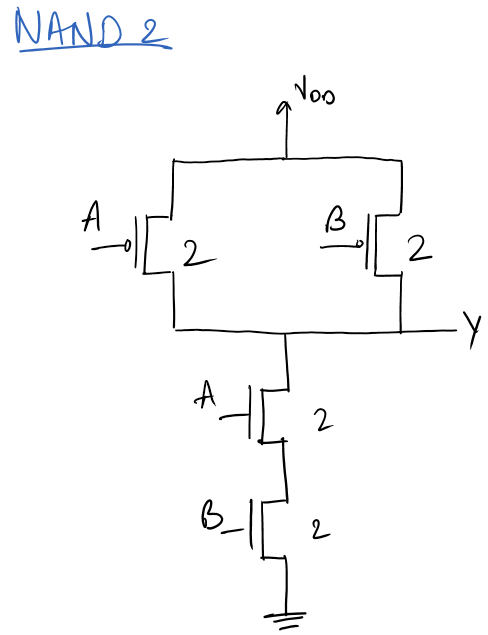
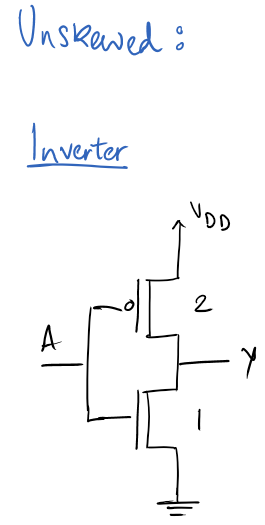
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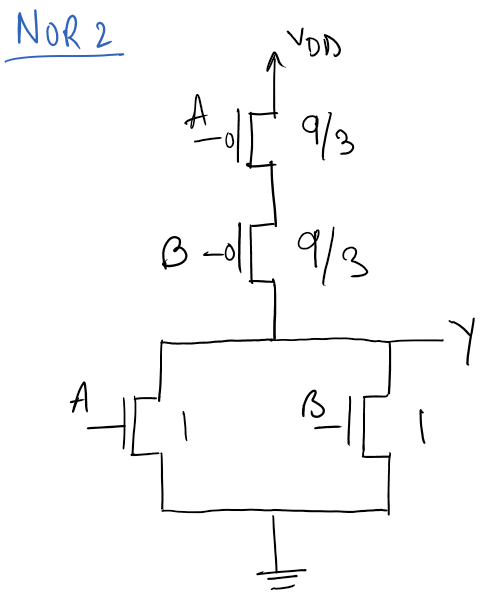
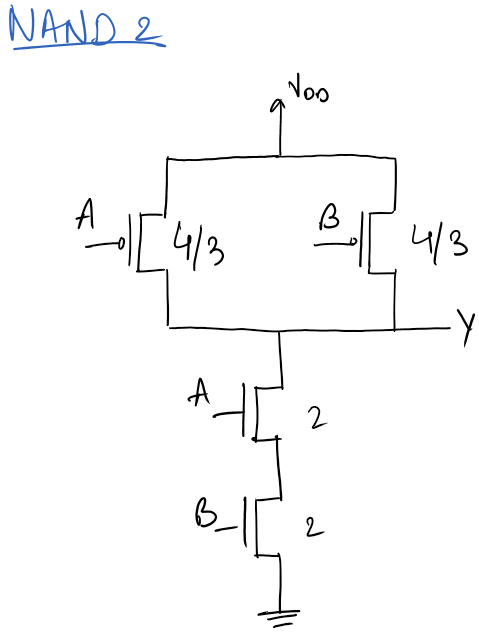
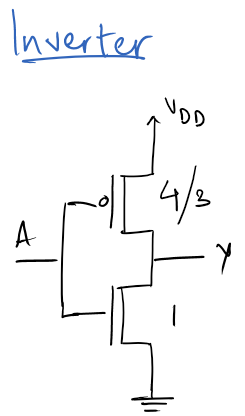
# **1. Pre-Lab**

## 1.1.



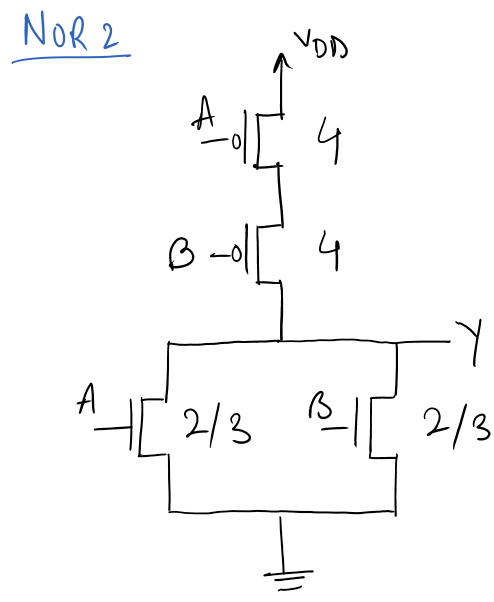
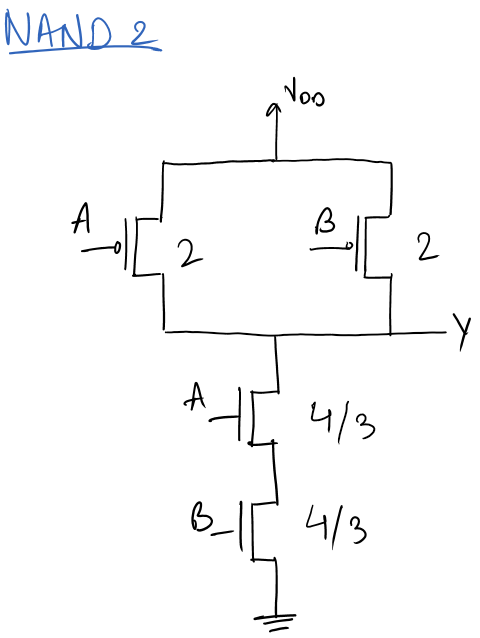
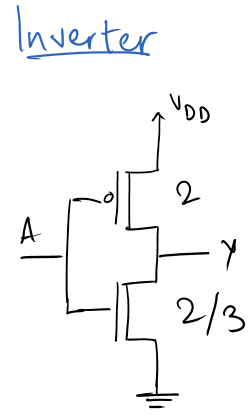
### *Figure 1: Unskewed: Inverter, NOR2 and NAND2 gates.*





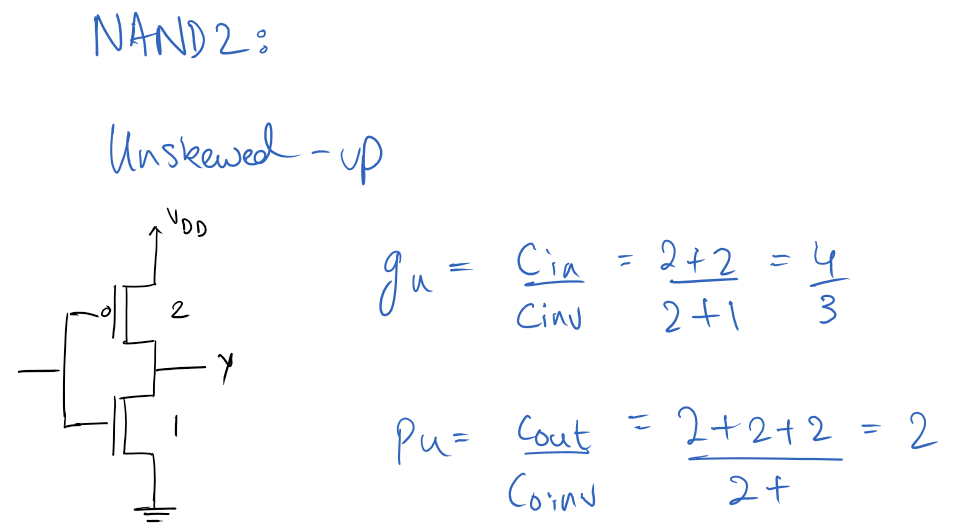
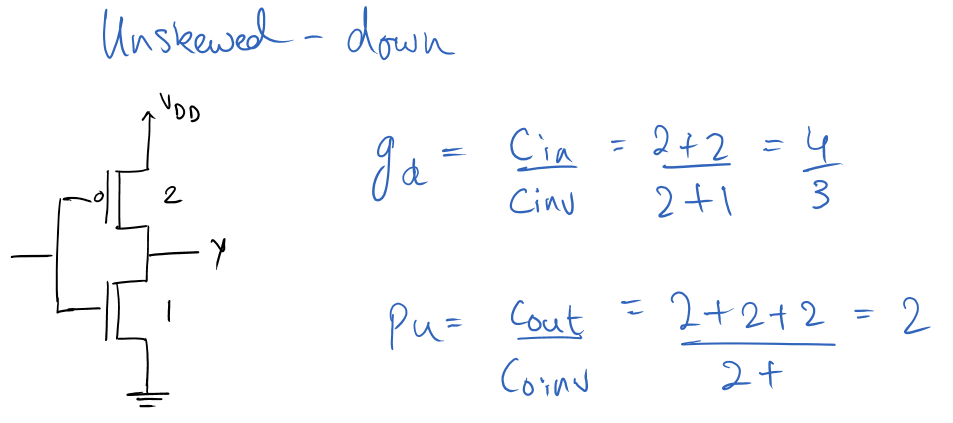
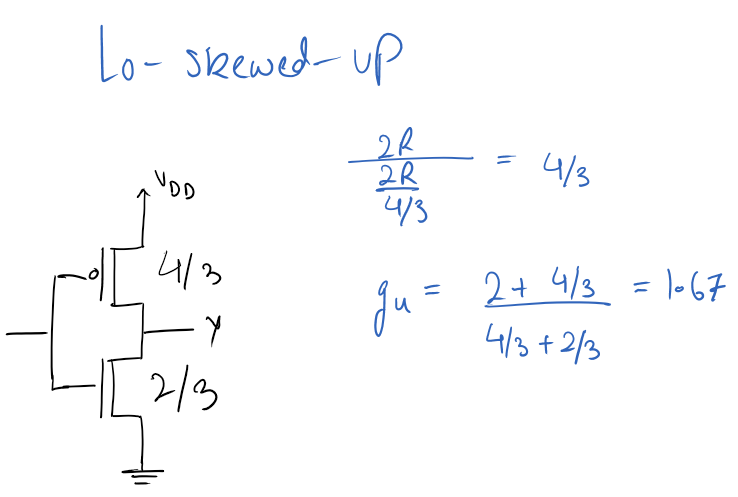
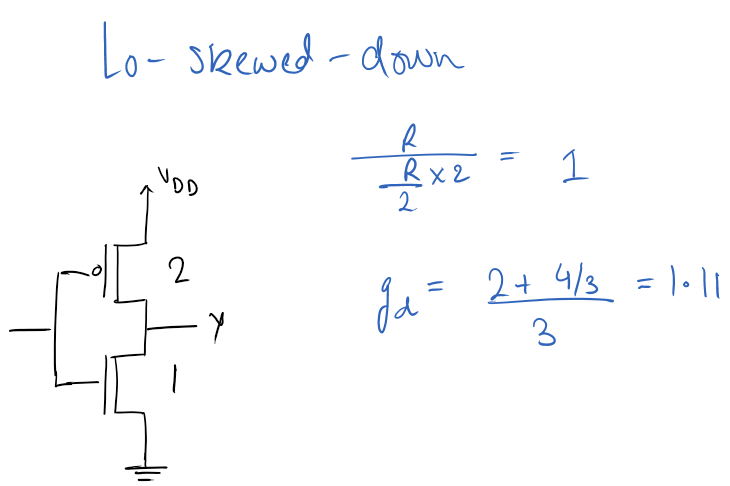
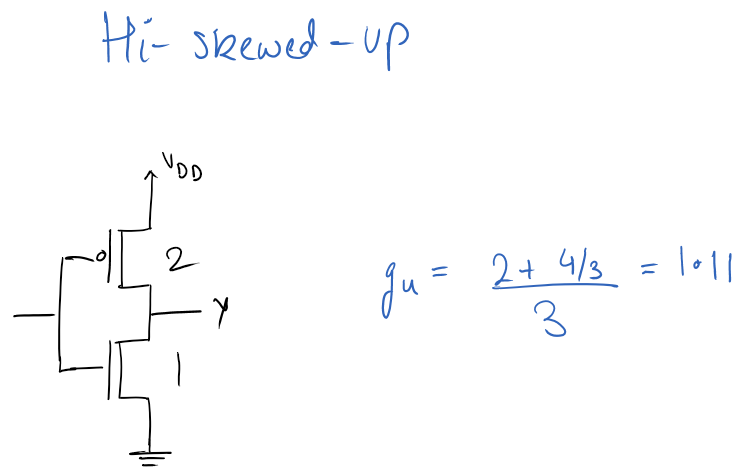
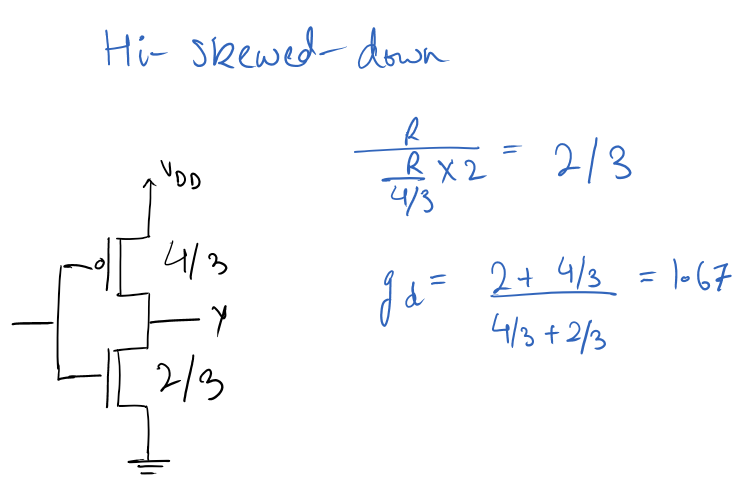
### *Figure 2: Low-skewed: Inverter, NOR2 and NAND2 gates.*

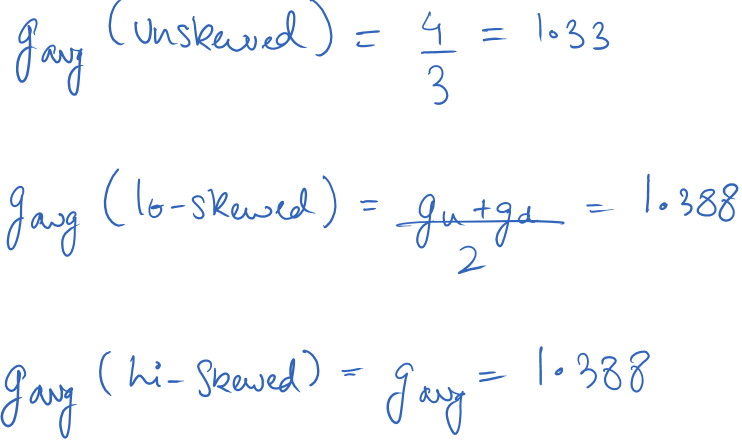




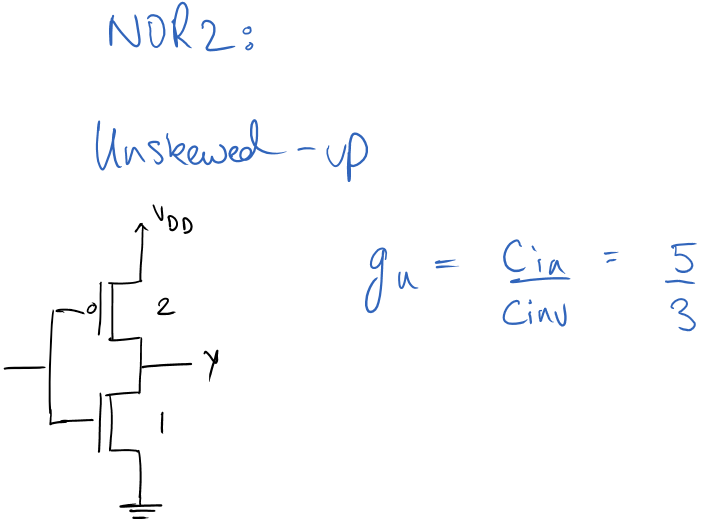
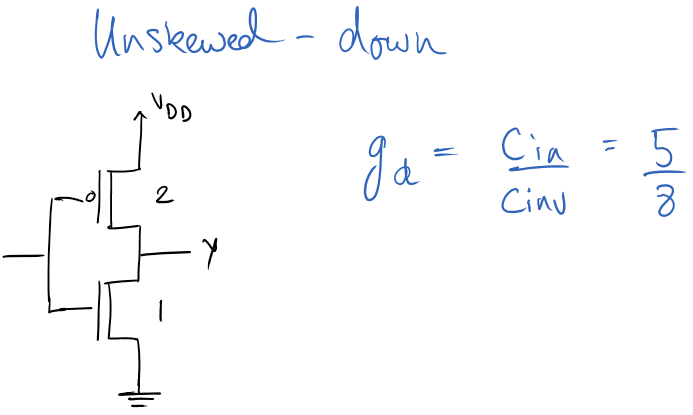
### *Figure 3: High-skewed: Inverter, NOR2 and NAND2 gates.*

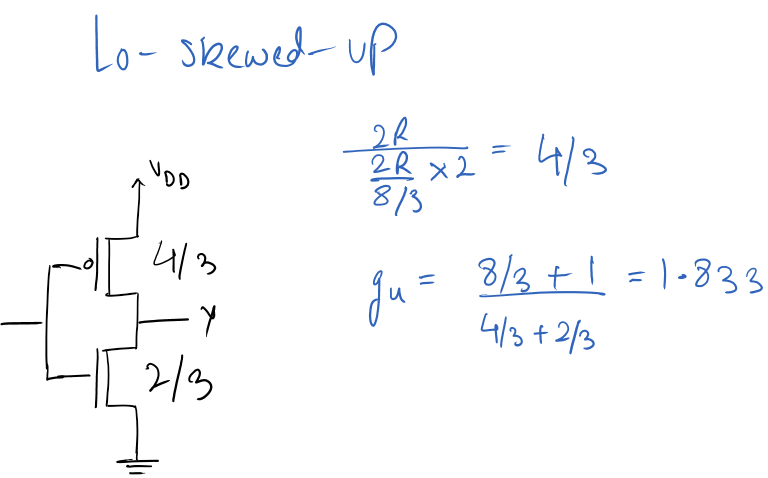
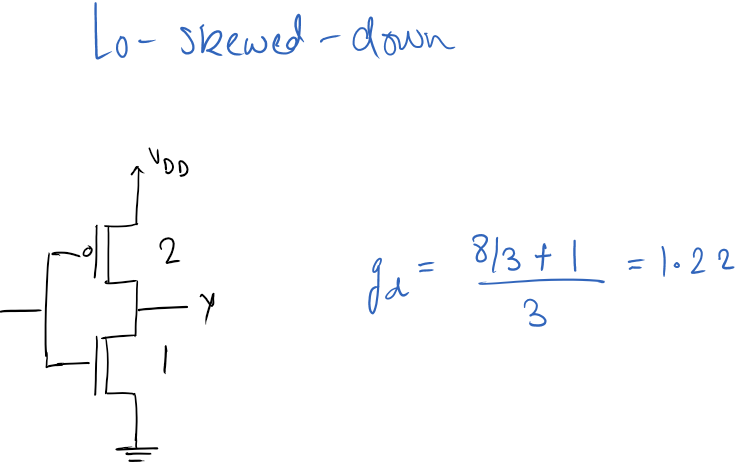
## 1.2

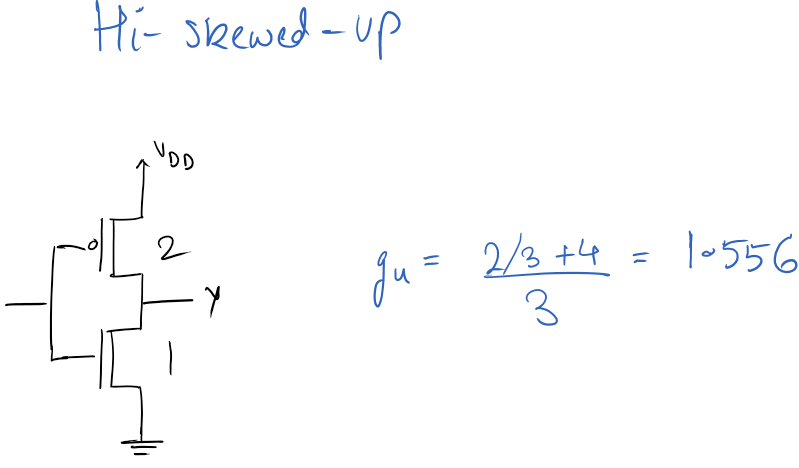
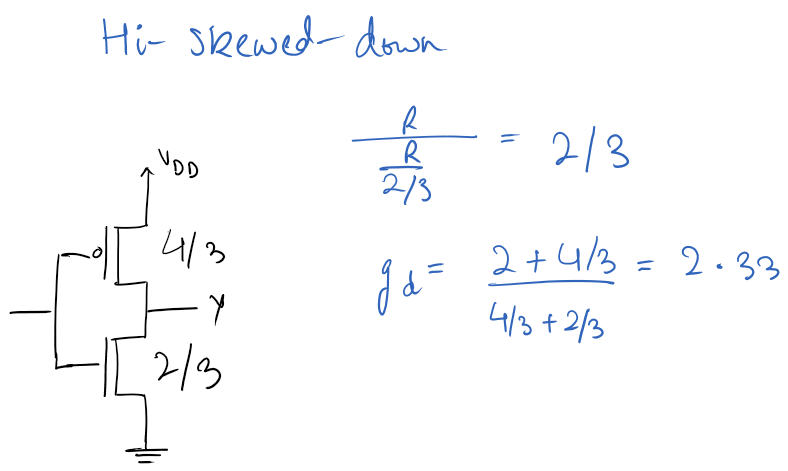
     

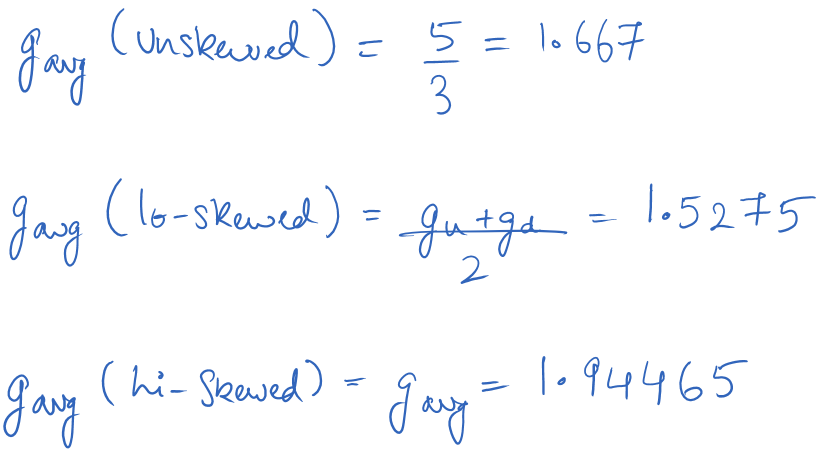


### *Figure 4: Rising, falling, and average logic effort for the unskewed, high-skewed and low-skewed NAND2 gate.*

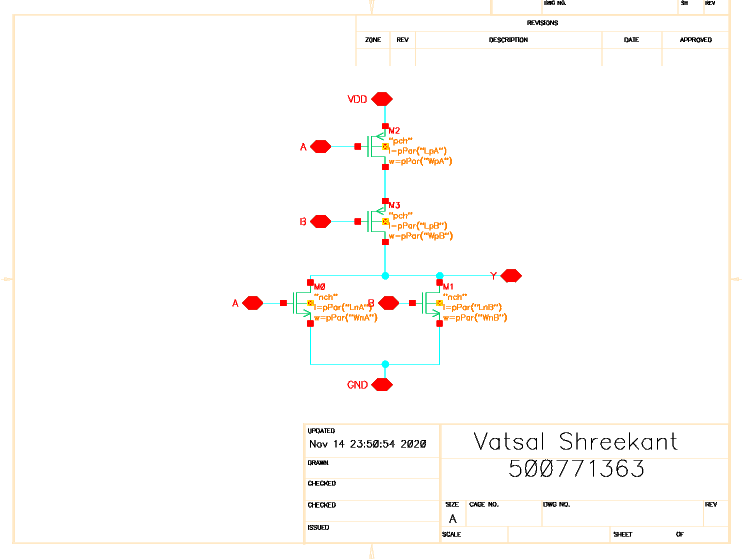
 



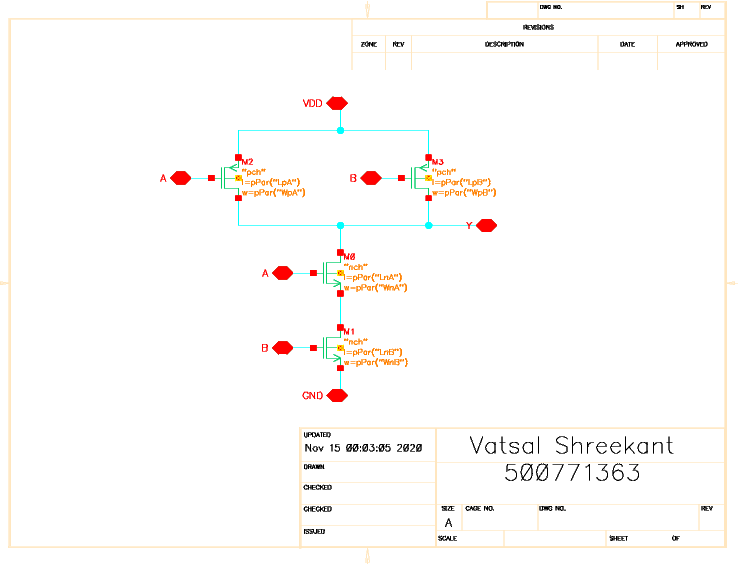
### *Figure 5: Rising, falling, and average logic effort for the unskewed, high-skewed and low-skewed NOR2 gate.*

# **2. Post-Lab**

## 2.1 Schematic of NOR2 and NAND2 gates

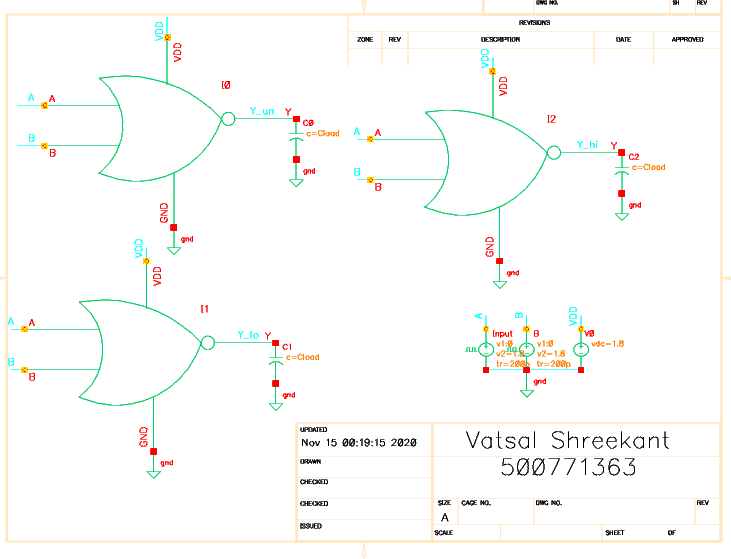


### *Figure 6: Schematic of NOR2 gate*

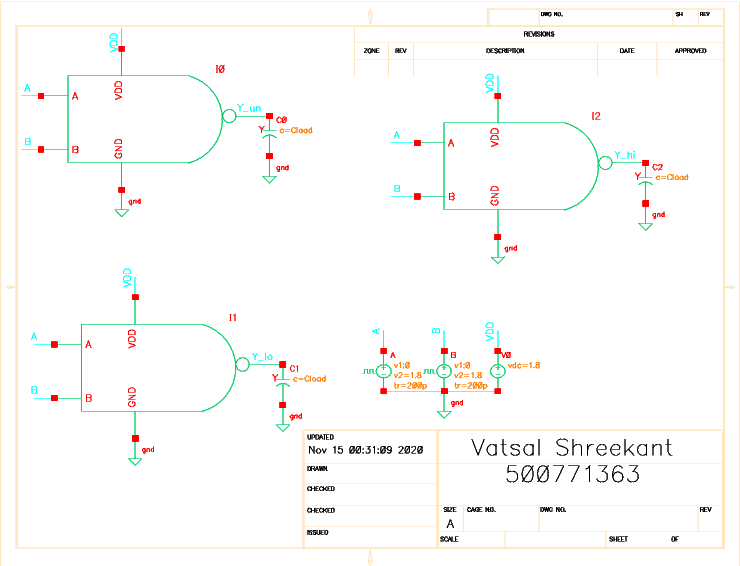


### *Figure 7: Schematic of NAND2 gate*

## 2.2 Schematic of Testbench of NOR2 and NAND2 gates

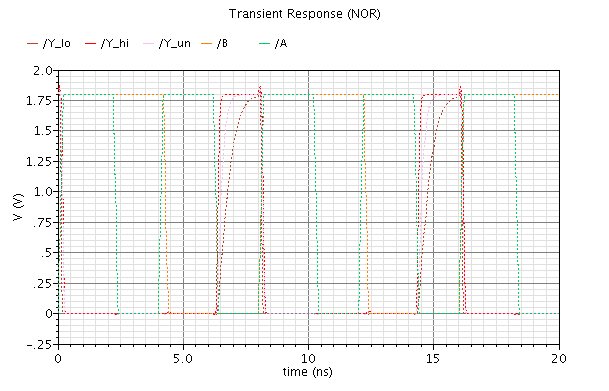


### *Figure 8: Schematic of NOR2 Testbench (skew testing)*



### *Figure 9: Schematic of NAND2 Testbench (skew testing)*

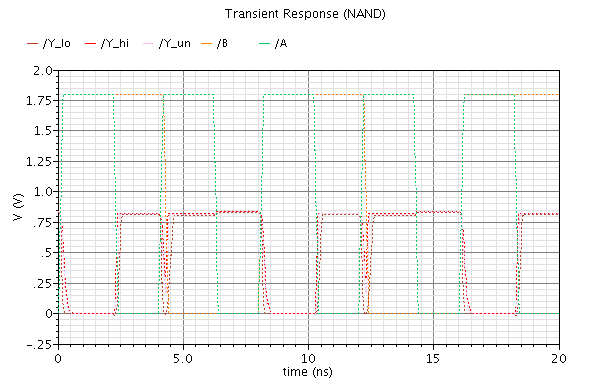
## 2.3 Delay measurement for unskewed, high-skewed and low-skewed NOR2 and NAND2 gates.



### *Figure 10: Schematic of NOR2 Transient Response*

### *Table 1: Delay Measurement for NOR2 (*unskewed, high-skewed and low-skewed*)*

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Unskewed** | **High-skewed** | **Low-skewed** |
| **Rising Delay (s)** | 94.01p | 73.37p | 121.63p |
| **Falling Delay (s)** | 93.89p | 100.25p | 89.63p |

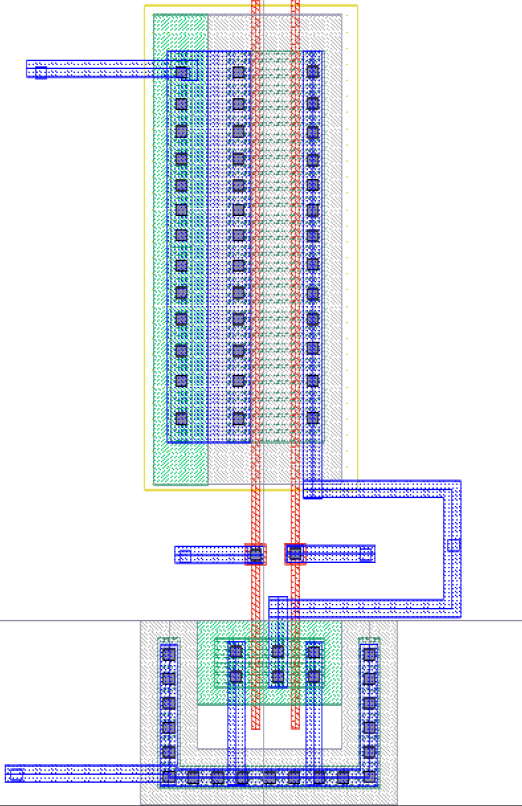


### *Figure 11: Schematic of NAND2 Transient Response*

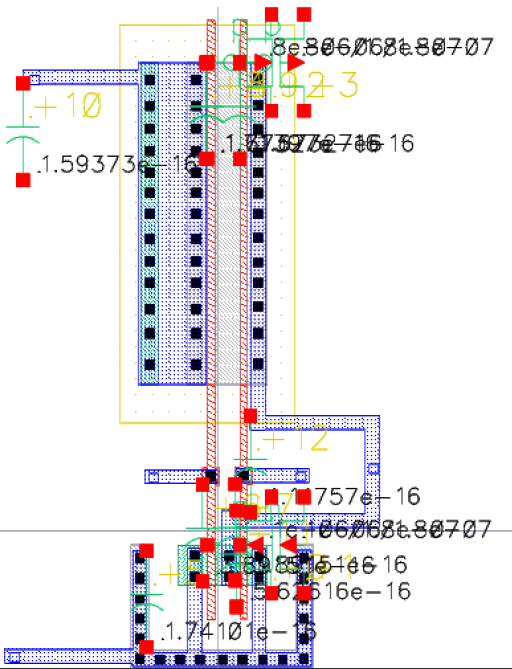
### *Table 2: Delay Measurement for NAND2 (*unskewed, high-skewed and low-skewed*)*

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Unskewed** | **High-skewed** | **Low-skewed** |
| **Rising Delay (s)** | 108.9p | 93.56p | 147.7p |
| **Falling Delay (s)** | 125.6p | 132.5p | 112.4p |

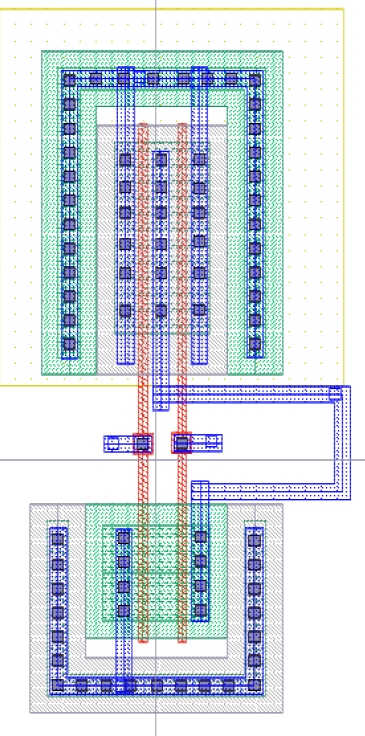
## 2.4 Layout and Extracted Views of the Unskewed NOR2 and NAND2 gates



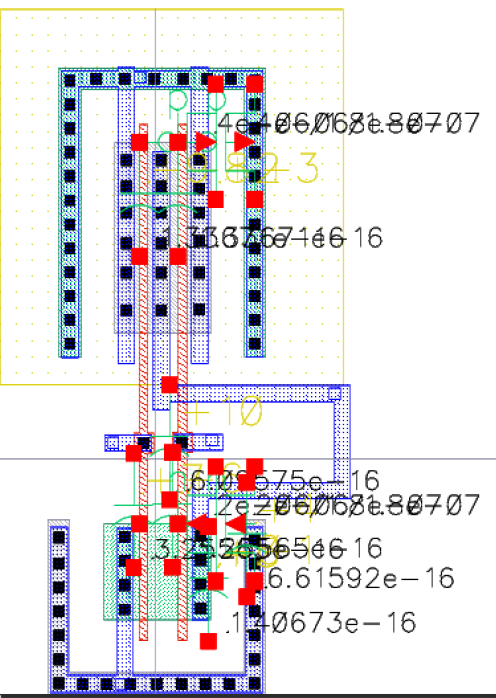
### *Figure 12: Layout View of NOR2*



### *Figure 13: Extracted View of NOR2*

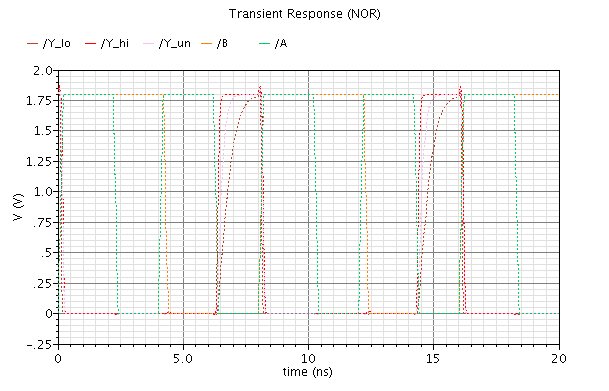


### *Figure 14: Layout View of NAND2*

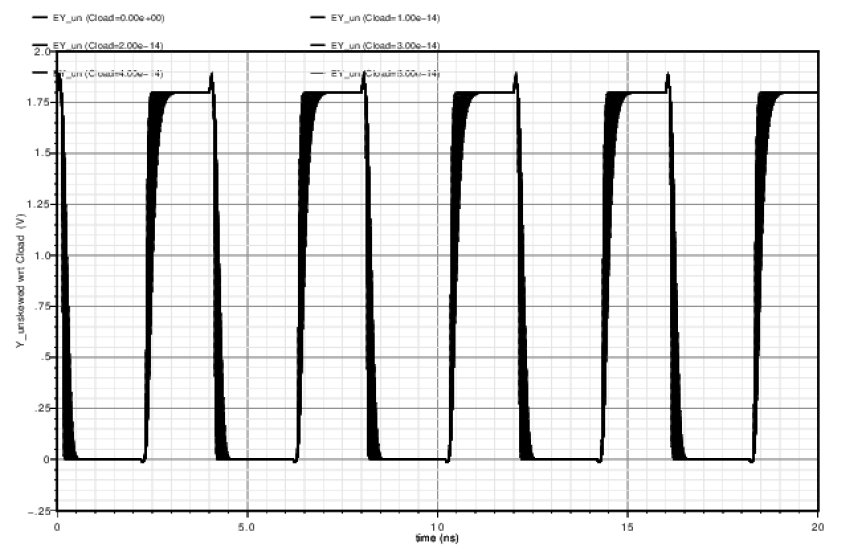


### *Figure 15: Extracted View of NAND2*

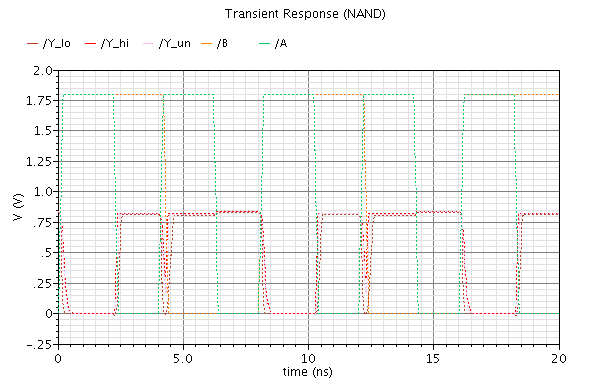
## 2.5 Post-layout simulation comparing delay measurement for unskewed NAND2 and NOR2 gates.



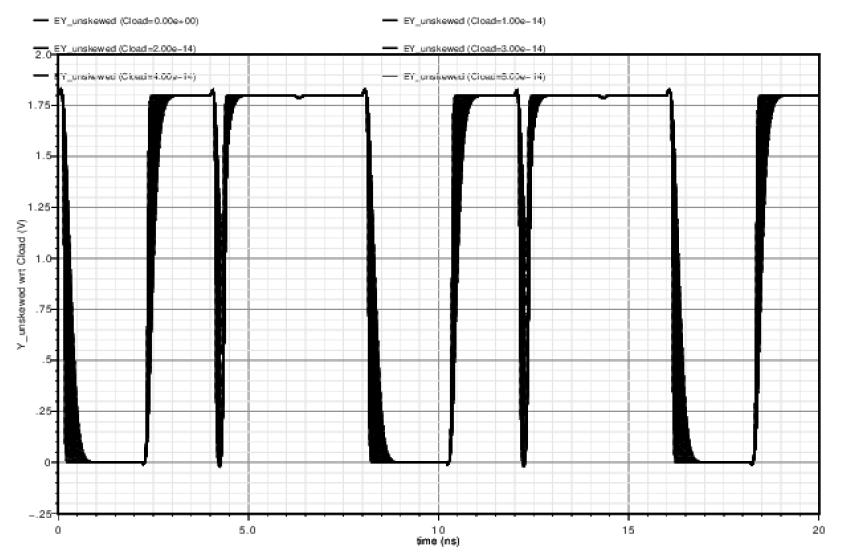
### *Figure 16: Unskewed NOR2 Transient Response*



### *Figure 17: Unskewed NOR2 Parametric Analysis*



### *Figure 18: Unskewed NAND2 Transient Response*



### *Figure 19: Unskewed NAND2 Parametric Analysis*

### *Table 3: Delay Measurement for NOR2 NAND2 (Schematic vs Extracted)*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **NOR2** | | **NAND2** | |
|  | **Schematic** | **Extracted** | **Schematic** | **Extracted** |
| **Rising Delay (s)** | 93.89p | 94.01p | 108.9p | 101.3p |
| **Falling Delay (s)** | 93.65p | 93.65p | 125.6p | 121.4p |

## 3 Conclusion

This lab explored different types of characteristics and the layout of a NOR2 and NAND2 gates. The static and dynamic simulations were performed through Transient and Parametric analysis. It was observed that the results obtained in the net list window were similar for both NOR2 and NAND2 testbenches. The deviations between extracted and schematic view was very low for the falling and rising delays. This can be seen when observing the results listed in Table 3. Thus, it can be assumed that this lab was successful in execution.